# Lab No.5)

**1)**

module dec2to4(W,En,Y);

input[1:0]W; input En; output [0:3]Y; reg [0:3]Y;

always@(W or En) begin if(En==1)

case(W) 0: Y=4'b1000;

1: Y=4'b0100;

2: Y=4'b0010; 3: Y=4'b0001; endcase else

Y=4'b0000; end

endmodule

module dec4to16(W,En,Y); input [3:0]W; input En; output [0:15]Y; wire[0:3]M;

dec2to4 dec1(W[3:2],En,M[0:3]); dec2to4 dec2(W[1:0],M[0],Y[0:3]); dec2to4 dec3(W[1:0],M[1],Y[4:7]); dec2to4 dec4(W[1:0],M[2],Y[8:11]); dec2to4 dec5(W[1:0],M[3],Y[12:15]); endmodule

module lab5\_1(W, En, f, g, h);

input [3:0] W;

input En;

output f, g, h;

wire [0:15]Y;

dec4to16 dec1(W, En, Y);

or(f, Y[3], Y[6], Y[7], Y[10], Y[11], Y[14]); or(g, Y[2], Y[3], Y[10], Y[14]);

or(h, Y[0], Y[1], Y[3], Y[7], Y[14], Y[15]);

endmodule

# 2)

module dec2to4(W,En,Y);

input[1:0]W;

input En;

output [0:3]Y;

reg [0:3]Y; always@(W or En) begin

if(En==1)

case(W)

0: Y=4'b1000;

1: Y=4'b0100;

2: Y=4'b0010; 3: Y=4'b0001; endcase else

Y=4'b0000; end

endmodule

module lab5\_2(x, y, c\_in, sum, c\_out); input x, y, c\_in;

output sum, c\_out;

wire [0:3] dec0w; wire [0:3] dec1w; wire [0:3] dec2w;

dec2to4 dec0({1'b0, x}, 1'b1, dec0w); dec2to4 dec1({c\_in, y}, dec0w[1], dec1w); dec2to4 dec2({c\_in, y}, dec0w[0], dec2w);

or(c\_out, dec2w[3], dec1w[1], dec1w[2], dec1w[3]); or(sum, dec2w[1], dec2w[2], dec1w[0], dec1w[3]); endmodule

# 3)

module dec2to4(W,En,Y);

input[1:0]W; input En; output [0:3]Y; reg [0:3]Y;

always@(W or En) begin if(En==1)

case(W)

0: Y=4'b1000;

1: Y=4'b0100;

2: Y=4'b0010; 3: Y=4'b0001; endcase else

Y=4'b0000; end

endmodule

module dec3to8(W,En,Y); input [2:0]W; input En; output [0:7]Y;

wire[0:3]M;

dec2to4 dec1({1'b0, W[2]},En,M); dec2to4 dec2(W[1:0],M[0],Y[0:3]); dec2to4 dec3(W[1:0],M[1],Y[4:7]); endmodule

module lab5\_3\_1(W, En, f, g, h);

input [3:0] W;

input En;

output f, g, h;

wire [0:7] temp0; wire [0:7] temp1; wire [0:7] temp2; wire [0:7] temp3; wire [0:7] temp4;

dec3to8dec0({1'b0,3],

W[2]}, En, temp0);

dec3to8 dec1({1'b0, W[1], W[0]}, temp0[0], temp1);

dec3to8 dec2({1'b0, W[1], W[0]}, temp0[1], temp2);

dec3to8 dec3({1'b0, W[1], W[0]}, temp0[2], temp3);

dec3to8 dec4({1'b0, W[1], W[0]}, temp0[3], temp4);

or(f, temp1[2], temp2[0], temp2[3], temp3[1]); or(g, temp1[0], temp1[3], temp4[3]);

or(h, temp1[0], temp1[2], temp3[2], temp4[0]); endmodule